Design Space Exploration for Interfacial-Layer-Free Negative-Capacitance FET

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Abstract

Negative-capacitance FET (NCFET), by utilizing a HfO_2-based ferroelectric gate stack, is a promising device candidate that may enable the downscaling of effective oxide thickness (EOT) and supply voltage (V_{DD}) for future logic devices [1]-[4]. The NC effect is based on the Landau-Khalatnikov (L-K) equation which describes a single-crystalline ferroelectric, and a hysteresis-free NCFET relies on the depolarization field stemming from the interfacial layer (IL) between the ferroelectric and the semiconductor channel. To achieve a single-crystalline-like ferroelectric, epitaxial growth of the ferroelectric directly on the semiconductor substrate is a promising approach [5][6]. In this work, we have explored the feasibility and hysteresis-free design space for interfacial-layer-free (IL-free) negative-capacitance FET (NCFET) based on the recently reported S-curve characteristic for ultrathin ferroelectric (1.5 nm) [7]. Our study indicates that, in the absence of an actual IL, the quantum-mechanical dark space near the Si surface (~0.4 nm EOT_e) can serve as the role of physical IL, allowing the short-channel NCFET to remain hysteresis-free for ultrathin ferroelectric with thickness less than 3.5 nm. This research is beneficial for future negative-capacitance devices using epitaxial technology.

Keywords -Negative-capacitance FET (NCFET), Interfacial layer

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