Conformal bilayer *h*-AlN epitaxy on WS_2 as an interfacial layer with ultralow leakage current

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Abstract

In this study, we developed an ultrathin epitaxial *h*-AlN interfacial layer (IL) between HfO_2 and a monolayer WS_2 channel using atomic layer deposition (ALD). Overcoming the challenge of growing ultrathin dielectrics on the dangling-bond-free surface of 2D materials, we employed sub-1 nm *h*-AlN as the IL and deposited HfO_2 high-k dielectric, achieving a uniform and atomically flat gate dielectric without voids. The resulting structure exhibited an equivalent oxide thickness (EOT) as low as 1 nm and ultra-low leakage currents of approximately 10^{-6} A/cm². The fabricated top-gate WS_2 transistors demonstrated on-off ratios around 10^6 and a subthreshold swing as low as 93 mV/dec. Additionally, we verified the feasibility of using *h*-AlN IL in gate-all-around (GAA) structures.

Furthermore, we achieved h-AlN epitaxy by plasma-enhanced ALD (PEALD) below 200°C on monolayer transition metal dichalcogenides (TMDs), demonstrating that the *h*-AlN layered dielectric is an excellent IL with atomic flatness and a relatively high dielectric constant. Combined with 2.7 nm HfO_2, it yielded an EOT of 1 nm. The insertion of h-AlN significantly improved the coverage and smoothness of HfO_2, resulting in a gate dielectric with good subthreshold swing, narrow hysteresis, high on-off ratio, and ultra-low gate leakage current densities. These leakage currents are orders of magnitude better than those of traditional Si CMOS, meeting the high-performance and low-power requirements of contemporary technology roadmaps. We also demonstrated the application of layered h-AlN epitaxy in GAA structures with an IL thickness below 0.6 nm.

Our work introduces a CMOS-compatible low-temperature ALD process for integrating gate dielectrics, providing excellent thickness scalability and uniform coverage around monolayer WS_2 nanosheets. The combination of high-quality two-dimensional dielectrics and semiconductors will advance the development of future high-performance, low-power electronic devices, opening new avenues for TMD transistor gate dielectric deposition technology.

***Keywords - Gate stack, Atomic layer deposition, 2D materials, h*-AlN, Gate-all-around**