Optimizing WSe_2 Double Gate FETs with Low-Temperature PE-AlN/TH-HfO_2 Gate Dielectrics and Post-Annealing Treatment

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Abstract

In this study, we demonstrate the successful integration of a low-temperature (100 °C) plasma-enhanced atomic layer deposition (PE-ALD) of AlN and TH-HfO_2 as gate dielectrics on WSe_2-based field-effect transistors (FETs). Initially, the device characteristics exhibited a transition from p-type to n-type behavior. To enhance the device performance without causing any damage, a post-deposition annealing process was carried out at 200 °C within a glove box environment. The annealing process effectively improved the device characteristics, confirming that the chosen temperature did not adversely affect the device. Subsequent double gate measurements were conducted, revealing that the low-temperature deposited AlN+HfO_2 dielectric stack maintained an equivalent oxide thickness (EOT) as low as 1 nm while preserving the functional integrity of the WSe_2 double gate device.

Keywords - WSe_2, PE-ALD, AlN