Monolithic Hybrid-3D Standard Cell Library with Sandwiched Inter-Metal Layer for 3D Digital Computation-in-Memory Circuits

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Abstract

In this aera of ever-shrinking hardware, the goal is to reduce transistor sizes to 2nm or even below 1nm. However, according to Moore's Law, we are approaching the physical limit of transistor miniaturization. To sustain Moore's Law, simply reducing transistor size isn't enough; breakthroughs must involve both improved structural design and the development of three-dimensional transistors.

We propose the use of Monolithic 3D (M3D) integrated circuits, which differ from TSV (Through-Silicon Via) 3D-IC technology. M3D stacks different layers sequentially on the same wafer and uses TVIA to connect Middle-end-of-line (MEOL) FinFETs with Front-end-of-line (FEOL) FinFETs, enabling true three-dimensional integration. The overall structure of these 3D integrated circuits comprises stacked FEOL FinFETs, M0, and MEOL FinFETs. MEOL and FEOL are pivotal in creating many 3D standard cells and circuits.

We employ Elevated-Laser-Liquid-Phase-Epitaxy (ELLPE) technology to reduce leakage current and circuit variability. ELLPE maintains the direction (100) single crystal on the MEOL FinFETs circuit. This research leverages ELLPE technology to build a complete three-dimensional standard cell library, hybrid (homogeneous and heterogeneous) multi-gate logic cell stacking, and Digital Computation-In-Memory circuits using a 12T Latch.

Stacking hybrid multi-gate logic elements is advantageous for constructing a three-dimensional standard cell library. When cells with a small number of transistors are built in 3D, the efficiency of area reduction is poor due to the disruption of the shared drain and source. This inefficiency is more pronounced when the original cell area is small. Conversely, 3D single-gate logic cells are ideal for complex wiring requiring more than two metal layers. Therefore, using both three-dimensional single-gate cells and hybrid multi-gate logic cells can reduce circuit area by 43% while maintaining the same delay.

These findings demonstrate that Digital Computation-In-Memory circuits designed with hybrid M3D stacked FinFETs improve performance, power, and area (PPA) metrics, offering more flexible circuit design.

Keywords - Monolithic 3D-IC、Elevated-Laser-Liquid-Phase-Epitaxy、Single-Crystal、3D standard cell library、Digital Computation-In-Memory circuits