

Strain Evolution in SiGe Nanosheet Transistor Process Flow

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Abstract

The step-by-step strain evolution in the channel during the SiGe nanosheet integration process flow for pFETs is demonstrated using finite element analysis (FEA). The effect of device dimensions and defective (seamed) S/D is studied. After fin formation, the 0.77% compressive biaxial strain resulting from the lattice mismatch between Si_{0.8}Ge_{0.2} and Si substrate is observed. However, the strain_{xx} is gradually relaxed during the source/drain recess and the inner spacer cavity formation. A large strain_{xx} is obtained on the channel along the current direction after Si_{0.6}Ge_{0.4} S/D regrowth, increasing from 0.21% to 1.50% for defect-free S/D epitaxy. The compressive strain along the channel remains similar for different shapes of the S/D regrowth, with small variations between every channel. Decreasing the nanosheet width only leads to an insignificant increase in channel strain_{xx} until the nanowire structure is formed. Nevertheless, the scaled body thickness can enhance the channel strain_{xx} substantially with the 21.2% compressive strain_{xx} increase from t_{body}=5 nm to t_{body}=1 nm. The seamed S/D is also simulated with air gaps between the defective merged epitaxes, where the strain inversion behavior is observed. The hole mobility with SiGe channel is expected to have a 3.6X enhancement with 1.5% compressive strain_{xx} to mitigate the mismatch of the driving strengths between pFETs and nFETs.

Keywords - SiGe, strain, nanosheet (NS), gate-all-around, finite element analysis (FEA)